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1 **Decoding of parallel Reed-Solomon codes with applications to proc concatenated codes**
Krachkovsky, V.Yu.; Yuan Xing Lee
Information Theory, 1998. Proceedings. 1998 IEEE International Symposiun

Page(s): 55
[Abstract] [PDF Full-Text] **CNF**

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2 **A 200 MHz register-based wave-pipelined 64 M synchronous DRAM**
Ho-Jun Song; Jung-Pill Kim; Jae-Jin Lee; Jong-Hoon Oh; Seung-Han Ahn; Ii Hwang
Solid-State Circuits, IEEE Journal of , Volume: 32 Issue: 1 , Jan. 1997
Page(s): 92 -99

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1 **An 833 MHz 1.5 W 18 Mb CMOS SRAM with 1.67 Gb/s/pin**
Pilo, H.; Allen, A.; Covino, J.; Hansen, P.; Lamphier, S.; Murphy, C.; Traver,
P.
Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2
International , 2000
Page(s): 266 -267

[Abstract]   [PDF Full-Text]   **CNF**